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INTEGRATED OPTOELECTRONICS DEVICES

Field of the Invention

This invention relates to the field of optoelectronics, and in particular to a structure and method which permits integration of at least two optoelectronic devices on a single substrate.

Background of the Invention

Optical systems are currently the subject of a great deal of attention in telecommunications primarily due to their enormous information-handling capacity. A typical system includes, at the transmitter end, a source of light, such as a laser, a modulator for impressing information onto the light signal, and one or more optical amplifiers for amplifying the optical signal. The signal is usually transmitted by means of an optical fiber. At the receiver end, typically a photodetector such as a PIN diode or avalanche photodiode (APD) may be employed to convert the optical signal to an electrical signal. Of course, several other components, such as optical switches, circulators, and isolators may be employed.

For purposes of economy and size it is desirable to integrate as many devices as possible on a single substrate. For example, it is known to integrate a laser and modulator into a single device generally known as an Electroabsorption Modulated Laser (EML). It is also known to integrate a Distributed Bragg Reflection (DBR) laser, a modulator, a Semiconductor Optical Amplifier (SOA) and a monitor onto a single substrate. Normally, when integrating active device components (i.e., devices which provide optical gain), the devices are formed by Selective Area Growth (SAG) with modifications to the composition, thickness, or number of Quantum Well layers in the active regions of the various devices. In the case of two active devices, it is difficult to optimize the device characteristics and the butt joint which couples the two devices together. In the case of three or more devices, the problem of optimization becomes especially difficult.

It has been proposed to couple active devices in an integrated structure using a passive waveguide. (See, e.g., U.S. Patent No. 5,134,671 issued to Koren et al, and U.S. Patent No. 5,029,297 issued to Halemane, et al.) However, such devices provide coupling between waveguide and device in a vertical direction which can also be difficult to make since the waveguide needs to be formed in the same growth process as the active devices. It is generally more advantageous to provide a butt coupling between devices (i.e., the light coupling is done in a horizontal direction) so that the coupling is optimized independently from the active devices.

It is desirable, therefore, to provide an integrated optoelectronic device with at least two active components where device characteristics and butt joint coupling may be optimized.

Summary of the Invention

The invention in accordance with one aspect is an optoelectronic device comprising at least two optical devices formed on a single semiconductor substrate, each optical device including an active region. The active devices are spatially separated and optically butt coupled by a passive waveguide formed on the substrate.

In accordance with another aspect, the invention is a method of forming an optoelectronic device comprising the steps of forming a plurality of epitaxial semiconductor layers on essentially the entire surface of a semiconductor substrate, the layers including at least one layer of an active material. The layers are then selectively etched to form spatially separate structures including the active material. An additional plurality of layers are then formed in the spaces between the structures, the additional layers including at least one passive waveguide layer so as to provide optical butt coupling between the active material of the separate structures.

Brief Description of the Figures

These and other features of the invention are delineated in detail in the following description. In the drawing:

Fig 1 is a cross sectional view of one example of a prior art optoelectronic device;

Fig 2 is a cross sectional view of an optoelectronic device in accordance with one embodiment of the invention; and

Figs 3-8 are cross sectional views of the device of Fig 2 during various stages of manufacture in accordance with an embodiment of the method aspects of the invention.

It will be appreciated that, for purposes of illustration, these figures are not necessarily drawn to scale.

Detailed Description

One example of a prior art device is illustrated in Fig 1. Merely by way of illustration, the device includes three active devices, a laser, 10, a modulator, 11, and a semiconductor optical amplifier (SOA), 12, formed on a semiconductor substrate, 13. Many other components can also be included, such as photodetectors. Each device includes a cladding or combination of cladding and Separate Confinement layers, 14, formed on the surface of the substrate, 13, an active layer, 15, deposited on the cladding layer, and another cladding/SCL layer, 16, deposited on the active layer. Other layers typically used, such as buffer layers and contact layers, are not shown for the sake of clarity. It will also be appreciated that the active layer, 15, can comprise a single Multi Quantum Well (MQW) layer or a plurality of MQW layers separated by barrier layers (not shown) as known in the art. Electrodes, 16-18, are selectively formed over the device structures, and electrode 19 is typically formed over the opposite surface of the substrate.

Typically, such devices are formed by depositing the various layers by Selective Area Growth (SAG) techniques. Varying the shape or size of the mask along the substrate can produce variations in composition and/or thickness of the active layer, 15, in the device regions, 10, 11, and 12, with a single deposition resulting in the desired device performances. The deposition also results in butt joints, illustrated by lines 20-23, which provide horizontal coupling between the devices. Thus, the device of Fig 1 includes an active layer, 15, which constitutes the active regions of the individual devices, 10-12, as well as the interconnection between the devices (although the composition and/or thickness of the layer, 15, will be varied across the device structure). A problem with such a technique is the difficulty in finding a growth condition which will optimize all the devices, 10-12, as well as the butt joints, 20-23. This problem is especially acute when the active regions of the devices comprise one or more MQW layers, and the integrated device is intended for use at 10 Gbit for distances of at least 50 km or for use at 40 Gbit.

Fig 2 illustrates a device structure in accordance with an embodiment of the invention. Again, the device, 30, includes a laser, 31, a modulator, 32, and an SOA, 33, integrated onto a single substrate, 33. As before, each component, 31-33, comprises a cladding/SCL layer, 35, an active layer, 36, and another cladding/SCL layer 37. However, rather than provide interconnection of the components by means of an active waveguide, the interconnections are made by a structure, 41 and 42, which includes a passive waveguide layer, 43. In this particular example, the passive waveguide layer, 43, is sandwiched between SCL layers, 44 and 45. In a preferred embodiment, the layers 43-45, can be formed sequentially in all the areas between components at the same time, i.e., the same layers will comprise the interconnections between all

components. The device, 30, also preferentially includes a layer, 46, formed over essentially the entire substrate surface. The layer comprises a composition, such as InGaAsP, which can perform the function of a stop etch in the processing to be described.

Another distinction in the device of Fig 2 is the fact that the active and cladding/SCL layers of any component, 31-33, are not necessarily formed at the same time as the corresponding layers of any other component, and, therefore, can be independently optimized.

It should be appreciated that one of the advantages of the structure of Fig 2 is that the butt joints, 50-54, formed by the passive waveguide layer, 43, and SCL layers, 44 and 45, can be optimized independently from the optimization of the active regions of the components, 31-33. Further, since the passive waveguide layer is typically undoped, improved electrical isolation and reduced optical loss can be achieved.

It should be understood that in the context of the present application, an active waveguide layer is considered to be any semiconductor layer which will generate light or absorb light in response to an applied bias. A passive waveguide layer is considered to be any semiconductor layer which will channel the light without generating any light or absorbing any significant amount of the light (less than 0.1dB loss).

Figs 3-8 illustrate a sequence of steps which can be performed in accordance with an embodiment of the method aspects of the invention in order to produce the device of Fig 2. In this particular example, all semiconductor layers are formed by Metal Organic Chemical Vapor Deposition (MOCVD), but other known techniques can be employed.

As illustrated in Fig 3, the substrate in this example comprises InP. Formed over essentially an entire major surface of the substrate is a stop etch layer, 46, which in this example comprises InAlAs or GaInAlAs. Any material which performs the stop etch function to be described can be employed. The layer, 46, is typically 0.1 to 0.5 microns thick. Formed on the stop etch layer, 46, is a combined cladding/SCL layer, 35. In this example, the layer, 35, comprises an n-type layer of InP with a thickness in the range 0.02 to 0.3 microns, and an n-type layer comprising InGaAsP with a thickness in the range 0.02 to 0.05 microns. The former layer is a standard cladding layer, and the latter is a standard SCL layer.

Formed on the cladding/SCL layer, 35, is an active layer, 36, which in this example is a multi-quantum well layer comprising InGaAsP layers of different composition so as to form layers of active quantum well material separated by barrier layers according to principles well

known in the art. The layer, 36, is typically undoped (intrinsic). The typical thickness of the layer, 36, is 0.09 to 0.2 microns.

A second cladding/SCL layer, 37, which is similar to the layer, 35, but with p-type conductivity, is formed on the active layer, 36. In this example, the layer, 37, includes a cladding layer comprising InP with a thickness within the range 0.2 to 0.7 microns, and an SCL layer comprising InGaAsP with a thickness within the range 0.02 to 0.10 microns.

A mask, 60, is then formed on the surface of the layer, 37, by first depositing a suitable material, such as silicon dioxide, and then patterning the material by standard photolithographic techniques.

The portions of the semiconductor layers, 35-37, which are exposed by the mask, 60, are then etched such that the final etching stops on layer 46 as illustrated in Fig 4. An etchant, such as $HCl:H_3PO_4$ is used so that layer 46 is not substantially etched.

Next, as illustrated in Fig 5, a new cladding/SCL layer, 35', active layer 36', and cladding/SCL layer, 37' are sequentially formed in the etched out areas. These layers, 35'-37' are essentially the same as the corresponding layers, 35-37, except that the composition and/or thicknesses are optimized for a modulator component (32 of Fig. 2) If desired, a new mask (not shown) can be formed to expose the area which will become the SOA component (33 of Fig 2), the exposed area etched, and then layers 35-37 regrown in the etched out areas to optimize the SOA device in a manner similar to the optimization of the modulator component. For the sake of exposition, it will be assumed that layers 35-37 are already optimized for laser and SOA components in the required areas.

Next, as illustrated in Fig 6, a second mask, 61, is formed over the surface of the structure of Fig 5. Again, the mask can be formed by depositing a layer of material such as silicon dioxide, and then patterning the layer by standard photolithographic techniques. In this step, the mask is patterned to expose the areas of the structure which will comprise the interconnection portions, 62 and 63, between the laser, modulator, and SOA components, as well as a portion, 64, at the edge of the device for coupling to some external component (not shown).

As illustrated in Fig 7, the portions of the structure exposed by the mask, are etched down to the stop etch layer, 46, i.e., layers 35,35', 36,36', and 37,37' are selectively etched. Again, the etchant employed could be $HCl:H_3PO_4$ or any other suitable wet or dry etchant which etches the layers without affecting the mask or the stop etch layer.

Subsequent to the etching step, as illustrated in Fig 8, layers 43-45 are sequentially grown to form the optical interconnection portions, 62 , 63, and 64 in the etched out areas. The mask, 61, can be used to provide selectivity in the growth process. In this example, the layers, 44 and 45, were SCL layers comprising InP, typically with a thickness in the range 0.005 to 0.6 microns. Layer, 43, sandwiched between the SCL layers was a passive waveguide layer comprising InGaAsP. The layers, 43-45 can be grown under conditions which optimize interconnection independently of the conditions for optimizing the device components. For example, the passive waveguide must be aligned to the two dissimilar device active regions such that low loss mode transfer occurs.

The mask. 61, can then be removed, and the structure completed by depositing the necessary electrodes to the top and bottom surfaces of the structure and cleaving the structure according to standard techniques to produce the device depicted in Fig 2.